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EXAMINER	
ELLIS, RICHARD L	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/390,079	KERR ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *67-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *67-117* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 67-117 are newly presented for examination.

2. The following in a quotation of the first paragraph of 35 USC 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 117 is rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, i.e., as lacking adequate written description.

Claim 117 claims a computer readable media that contains instructions for execution by a processor, and that the instructions are to 1) provide a multiplexer having particular inputs and outputs, and 2) couple the multiplexer inputs and outputs to an ALU. However, applicant's specification is silent as to how execution of an instruction within a processor will "provide" ("to supply or make available" - *Webster's Ninth New Collegiate Dictionary*, 1990) a multiplexer. The literal claim language is that the instruction supplies the physical multiplexer, however, and instruction is simply a collection of data bits that are interpreted by a processor, the instruction can not directly "provide" (supply or make available) any physical piece of hardware. Additionally, the claim is also claiming that the instruction literally couples the multiplexer to the alu, as in it physically routes/creates the metal wires necessary for the mux to be connected to the alu. For the same reason that an instruction can not supply or make available a physical piece of hardware, that same instruction can not also directly supply the metal wiring necessary to connect the mux to the alu. The specification is totally silent as to any discussion of the instruction physically supplying the multiplexer, and as to any discussion of the instruction physically creating the metal interconnecting wires between the multiplexer and the alu. Therefore, the specification does not contain an adequate written description of the invention claimed in claim 117.

4. Claim 117 is rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the discussion above, it was noted that the specification was silent as to an instruction performing a supply of physical elements (a mux and interconnecting wires). Because the specification is silent as to the instruction performing this feat, it is quite apparent that same silent specification can not enable one of skill in the art to make the invention where an instruction supplies physical hardware and physical metal wires. One of ordinary skill in the art would have to perform undue experimentation in order to make the invention claimed in claim 117. Accordingly, claim 117 is not supported by an enabling disclosure.

5. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

8. Claims 67-72, 78-97, and 104-117 are rejected under 35 USC § 102(b) as being clearly anticipated by Hao et al., U.S. Patent 4,594,655. .

Hao et al. taught (e.g. see figs. 1-4f) the invention as claimed (as per claim 67), including a data processing ("DP") system comprising:

A. a processor (fig. 1) comprising;

B. a first execution unit (1) having a first (5) and second (6) input register coupled to first (left side of element 2) and second (right side of element 2) inputs to a first arithmetic logic unit (ALU) (2), the first and second input registers of the first execution unit to store source operands (col. 9 line 66 to col. 10 line 4);

C. a second execution unit (21) having a first (25) and second (26) input register, the second register coupled to a second input (right side of element 22) to a second ALU (22), the first and second input registers of the second execution unit to store source operands; and,

D. a multiplexer (MUX) (mux shown just above the letter A at element 22) having i) a first input (dot and line to the mux) coupled (line traversing across the drawing to connect to elements 2 and 5) to the first input (left side of element 2) of the first ALU (2), ii) a second input (line without dot to the mux) coupled to the first input register (25) of the second ALU (22), and iii) an output (connection from mux to center of element 22) directly (there are no intervening elements between the mux and the ALU) providing a first input (middle input to element 22) to the second ALU (22), the MUX permitting both the first (2) and second (22) ALU to share (line connecting dot above mux to element 5) the source operand (S1) stored in the first input register (5) of the first ALU (2).

9. As to claims 92 and 111, they do not teach or define above the invention claimed in claim 67 and are therefore rejected under Hao et al. for the same reasons set fourth in the rejection of claim 67, supra.

10. As to claim 68, 93, and 112 Hao et al. taught an instruction set (col. 7 lines 16-34) defining a register decode value (col. 7 line 64, the register decode value is R3) that specifies source operand bypassing (col. 7 lines 63-64, presence of register decode value R3 in inst1 and in inst2 defines operand source bypassing) such that the MUX, in response to the register decode value that specifies source operand bypassing, selects the first input of the MUX coupled to the first input of the first ALU as the output of the MUX (col. 7 lines 65-66, presence of register decode value R3 results in ALU2 receiving R1 and R2, the same values supplied to ALU1, therefore, R1 and R2 have been source operand bypassed), the output of the MUX providing the first input to the second ALU (connection from mux to center of element 22).

11. As to claims 69, 94, and 113, Hao et al. taught that the source operand bypassing value allowed the second execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first execution unit (col. 7 line 66 to col. 8 line 6, in Ex. 2, inst I1 calculates an effective memory address, and inst I2 retrieves the data at the calculated memory address).

12. As to claims 70, 85, 95, and 114, Hao et al. taught a local bus (lines between 23, 7, 3, and 8, 9) for communicating with a memory (8, 9), a register file (4, 24) for storing intermediate operands; and, an instruction decode stage (12) for coupling the register file to the first and second input registers of the first and second ALUs to provide intermediate operands as the source operands, and for coupling a memory bus to the first input register of the of the first ALU to provide source operands from the memory (8, 10, 11, 4, 24).

13. As to claims 71, 96, and 115, Hao et al. taught that the first input register (5) of the first ALU (2) provided source operands from the memory (8, 10, 11, 4) to both the first input to the first ALU (left side of element 2) and to the first input of the MUX (line from 5 to dot at mux), thereby permitting the first input to the second ALU (middle input of element 22) to share the source operands from the memory directly from the first input register of the first ALU (line from 5 to ALU 2 and 22 allows sharing the data value between the two ALU's).

14. As to claims 72 and 97, Hao et al. taught a pipeline of the processor (col. 4 lines 66-68), the pipeline having a plurality of stages including instruction decode, writeback, and execution stages (col. 1 lines 36-44), the execution stage having the first and second execution units (col. 9 lines 30-49).

15. As to claim 78, Hao et al. taught an instruction set (col. 7 lines 16-34) defining a register decode value (col. 7 line 64, the register decode value is R3) that defines source operand bypassing (col. 7 lines 63-64, presence of register decode value R3 in inst1 and in inst2 defines operand source bypassing) that allows source operand data to be shared among the first and second execution units by directly addressing a source register of the first execution unit (col. 7 lines 65-66, presence of register decode value R3 results in ALU2 receiving R1 and R2, the same values supplied to ALU1, therefore, ALU2 has directly

addressed a source register of the first ALU).

16. As to claim 104, Hao et al. taught defining a register decode value (col. 7 lines 61-65, the register decode value is R3) that defines source operand bypassing of source operand data (presence of R3 in inst 1 and inst 2 results in ALU1 receiving R1 & R2, and ALU2 receiving R1 & R2, therefore source operand bypassing of source operand data has occurred).

17. As to claim 105, Hao et al. taught identifying a pipeline stage register (5) for use as a source operand in an instruction (col. 7 lines 61-66, inst1 uses R1 and R2 which are staged into S1, S2 of fig. 1) containing the register decode value (instruction inst 1 contains the R1 and R2 register decode values) by directly addressing a source register (presence of R1 and R2 in inst 1 call for the system to access GPR's (4) to access the registers pointed to by R1 and R2 of inst 1).

18. As to claim 106, Hao et al. taught sharing source operand data among the first and second execution units of the pipelined processor through the use of a source bypass (RISB) operand in the register decode value (col. 7 lines 61-66, presence of a source bypass (RISB) operand (R3) in inst 1 and inst 2 results in R1 & R2 being shared between ALU1 and ALU2).

19. As to claim 107, Hao et al. further taught receiving data at the second execution unit, the data stored at a memory address specified by a displacement operand in a previous instruction executed by the first execution unit of the processor (col. 7 line 66 to col. 8 line 6, in Ex. 2, inst I1 calculates an effective memory address, and inst I2 retrieves the data at the calculated memory address).

20. As to claim 108, Hao et al. taught use of source operand bypassing as detailed at (col. 7 lines 61-65). Inherently, when inst 1 of Ex. 1 is a memory operation that reads into r3, and inst 2 accesses R3, the disclosed bypassing system would have provided for realizing two [apparent] memory references with a single bus operation because inst 2 would share the value retrieved by inst 1 instead of repeating the memory operation specified by inst 1).

21. As to claim 109, Hao et al. taught sharing a source operand (S1) stored in a first input register (5) of the first ALU (2) at the first and second ALU (2, 22) substantially simultaneously (line from 5 to 2 and 22 carries value of S1 to both ALU's simultaneously).

22. As to claim 84, Hao et al. taught:

A. a first arithmetic logic unit (ALU) (2);

B. a second ALU (22);

C. a multiplexer (MUX) (mux above input A of ALU 22) having i) a first input (line with dot at mux) coupled to a first input of the first ALU (line with dot at mux extending over to connect to element 5 and input 1 of ALU 2), ii) a second input (line without dot at mux) coupled to source operands (25), and iii) an output (area beneath mux) providing a first input to the second ALU (the mux at A provides the middle input to ALU 22), the MUX permitting both the first and second ALU to share the same source operand (when the first input (line with dot) is selected by the mux, the source operand from 5 is shared between both ALU 2 and 22); and,

D. an instruction set (col. 7 lines 16-34) defining an instruction (col. 7 lines 21-34) that when decoded operates the MUX to permit both first and second ALUs to share the same source operand (col. 7 lines 64-66, ALU1 receives R1 & R2, ALU2 also receives (shares) R1 & R2).

23. As to claim 86, Hao et al. taught a register decode value of the instruction set (col. 7 line 64, the register decode value is R3) that defines source operand bypassing (col. 7 lines 63-64, presence of register decode value R3 in inst1 and in inst2 defines operand source bypassing) that allows source operand data to be shared among the first and second ALUs by directly addressing a source register of the first ALU (col. 7 lines 65-66, presence of register decode value R3 results in ALU2 receiving R1 and R2, the same values supplied to ALU1, therefore, ALU2 has directly addressed a source register of the first ALU).

24. As to claims 79 and 87, Hao et al. taught that the source operand bypassing value allowed the second ALU to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first ALU (col. 7 line 66 to col. 8 line 6, in Ex. 2, inst I1 calculates an effective memory address, and inst I2 retrieves the data at the calculated memory address).

25. As to claims 80 and 88, Hao et al. taught a register file (4, 24) containing a plurality of general-purpose registers (4, 24) for storing intermediate result data processed by the first and second execution units (col. 5 lines 52-65 and col. 6 lines 20-32).

26. As to claim 81 and 89, Hao et al. taught that the first and second execution units were parallel execution units (col. 7 lines 14-15 and col. 10 lines 11-14).

27. As to claim 82 and 90, Hao et al. taught a current execution unit (1) as the first execution unit; and, an alternate execution unit (21) as the second execution unit.

28. As to claims 83, 91, 110, and 116, Hao et al. taught that the first and second ALU share the source operand stored in the first input register of the first ALU substantially simultaneously (col. 12 lines 34-44).

29. As to claim 117, Hao et al. taught a computer readable media (fig. 1, 9) containing instructions (13, 14) for execution by a processor (fig. 1) for the method of providing a mux (mux above middle input to ALU2) having first and second mux input (line with dot and line above A above ALU2 middle input) and a mux output (connection between mux and middle input of ALU2); coupling the first mux input to a first input of a first ALU (line without dot connected to element 26), coupling a second mux input to a first input register of a second alu (line with dot connected to element 5, which is input to ALU1); and, directly providing, by the mux output, a first input to the second ALU, the MUX permitting both the first and second ALU to share a source (line with dot above mux connects to element 5 to transmit the contents of element 5 to the mux for selection into the input of ALU2) operand (S1) stored in a first input register (5) for the first ALU (2).

30. Claims 73-77 and 98-103 are rejected under 35 USC § 103 as being unpatentable over Hao et al., U.S. Patent 4,594,655, as applied to claims 67-72, 78-97, and 104-116, in view of Asato, U.S. Patent 6,145,074.

31. As to claims 73 and 98, Hao et al. did not teach an instruction set defining a register decode value that defines result bypassing that allows bypassing of a result from a previous instruction executing in pipeline stages of the processor by directly addressing a result register of the first and second execution units. However, Asato taught an instruction set (fig. 5) that

defined a register decode value (b1, b2, p1, p2) that defines result bypassing (fig. 1, bp1, bp2) that allows bypassing of a result from a previous instruction executing in pipeline stages (2) of the processor by directly addressing a result register of the first and second execution units (fig. 4, 21-1, 21-2, 21-3, 21-4, fig. 12, bp1, 51, bp2, 52, bp3).

32. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Asato's instruction set defining result bypassing system into Hao et al.'s source bypassing system because of Asato's teaching that result bypassing allows for faster execution of certain instruction combinations as compared to no result bypassing (col. 2 lines 14-22) and Hao et al.'s teaching that it is desirable to accelerate execution of certain instruction combinations (col. 4 lines 53-65). Additionally, both Hao et al. and Asato indicate that their respective systems impose only a small additional hardware burden upon the system (Hao et al. at col. 4 lines 62-65 and Asato at col. 2 lines 53-57).

33. As to claim 74, Asato taught both inter-unit result bypass (fig. 5, fig. 7) as well as result bypass as detailed supra.

34. As to claim 75, Asato taught that the RRB denoted all execution units (fig. 1, b1, b2, fig 2, 5, 6, 2, fig. 5, b1, b2, p1, p2, fig. 7) which includes the first unit, and taught that the RIRB denoted another unit, which includes a second unit (fig. 7).

35. As to claim 76, Asato taught that the RRB operand explicitly infers feedback (fig. 2, 9, 10) of the data delivered from the first execution unit (fig. 2, 2) to an input register of the first execution unit (3, 4) over a feedback path (9, 10).

36. As to claim 77, Asato taught that the write back stage comprised an interstage register (fig. 12, 52) and wherein the RRB operand enabled bypassing write-back of the data processed by the first and second execution units to one of the register file or the inter-stage register of the writeback stage (fig. 2, 9, 10, 13).

37. As to claim 99, Asato taught identifying a pipeline stage register (fig. 12, 51, 52) for use as a source operand in an instruction containing the register decode value by directly addressing a result register (bp1, bp2, bp3).

38. As to claim 100, Asato taught explicitly controlling data flow (fig. 2) within the

pipeline stages of the processor (2) through the use of a register result bypass (RRB) operand in the register decode value (fig. 1, b1, b2).

39. As to claim 101, Asato taught retrieving data from the first execution unit (fig. 7, "From 21-1"), and returning the data to an input of the first and second execution registers ("to pipeline register 3", "to pipeline register 4") of the first and second execution units (fig. 6, 21-1, 21-2, 21-3, 21-4) as specified by the RRB operand (fig. 5, b1, b2, p1, p2), thereby bypassing write-back of the data to either a register file or memory at the writeback stage (22).

40. As to claim 102, Asato taught explicitly specifying the pipeline stage register to be used as the source operand for the instruction (fig. 1, b1, b2, fig. 2, bp1, bp2, fig. 5, b1, b2, p1, p2).

41. As to claim 103, Hao et al. taught encoding the RRB operand in fewer bits than a regular register operand (fig. 1, b1, b2 fields are smaller than s1, s2 fields, fig. 5, b1, b2, p1, p2 fields are smaller than s1, s2 fields).

42. Applicant's arguments with respect to claim 67-117 have been considered but are deemed to be moot in view of the new grounds of rejection.

43. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

44. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
May 26, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER